Radiation Tolerant Ultra Low Power CMOS Microelectronics: Technology Development Status

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***Abstract*- Electronic components used in spacecraft are susceptible to the radiation environment that causes detrimental effect which could jeopardize the mission. Much effort has been devoted to methodologies that would produce radiation tolerant or hardened devices hopefully with speed-power performance close to commercial parts. Recent development in combining radiation tolerance by design technique with ultra low power CMOS circuit technology promises dramatic impact on future NASA spacecraft. The measured performance at 0.5V demonstrates over 30:1 power reduction compared to a similar device with 3.3 V supply voltage. This paper gives a status report on the development of such radiation tolerant ultra low power electronics technology.**

I. INTRODUCTION

Ultra Low Power (ULP) electronics concept was conceived in the mid-90's [1]. The fundamental idea is to lower total power by reducing dynamic power associated with switching circuits which then enables a reduction in power supply. However, as the supply voltage decreases, the circuit also becomes more susceptible to radiation effects, problems especially of concern for space electronics. Without effective means to mitigate the radiation effect, the ULP circuits will not meet the requirement for space applications.

Fortunately, through the last 10 years of technology investment, NASA/GSFC has supported the development of a break-through technology at the U. of Idaho's (formally U. of New Mexico) Center for Advanced Microelectronics and Biological Research (CAMBR) This break-through, known as Radiation Tolerance (RT) by design technology, allows space electronics to be fabricated at commercial foundries. This feature is achieved solely from ingenious circuit design and layout techniques. As an example, a Application Specific Integrated Circuit (ASIC) performing channel error detection/correction at over 200 Mbps was implemented in RT, fabricated in a commercial foundry and flown on NASA missions such as HST, LANDSAT, TERRA, EO-1, MAP, etc. New designs are expected to exceed 1 Gbps.

By marrying the RT technology with the ULP concept, preliminary estimate points towards a potential of over 50% power savings for future spacecraft. Considering the difficulty and the cost associated with developing photo-voltaic technology to increase solar cell efficiency by merely a few percentage points, NASA simply cannot afford overlooking the potential payoffs the RTULP technology may provide.

II. RT AND ULP BASICS

A. RT CMOS

The development of radiation tolerant Complimentary Metal Oxide Semi-conductor (CMOS) Very Large Scale Integration

(VLSI) based upon the commercial Integrated Circuit (IC) industry has created the potential for major advances in space flight electronics[2,10]. The radiation tolerant technology has been demonstrated and is utilized in existing 5 volt flight chips[2,3]. Our approach operates on the principle of providing electronic feedback and additional guard-rings to compensate for the impacts of a cosmic particle strike, commonly known as single-event effects (SEE). The most critical single event effects in digital integrated circuits are single event upset (SEU), which temporarily changes the state of a memory cell, and single event latchup (SEL), a potentially catastrophic high-current state. RT technology allows flight engineers the ability to design and manufacture radiation tolerant devices using commercial foundries with commercial CAD tools at commercial technology schedules and prices [2].

There are two general approaches to meeting the need for electronic systems in high radiation environments. Radiation *tolerant* VLSI, achieved through design only, is fabricated in a commercial IC process without any special process steps oriented towards improving radiation hardness. Radiation *hard* VLSI is normally fabricated in a specialized foundry that executes special steps to enhance total dose radiation hardness, in addition to design methods. Table 1 compares the radiation resistance capabilities of radiation tolerant VLSI and radiation hard VLSI.

TABLE 1
RADIATION TOLERANCT AND RADIATION HARD

Radiation Effect	Radiation Tolerant	Radiation Hard
Total Dose (rad (Si))	> 50K	1 Meg
SEU LET (MeV · cm^2 /mg)	> 40	> 40
SEL LET (MeV · cm^2 /mg)	> 120	> 120

The primary advantages of radiation tolerant VLSI are:

- Flight VLSI can take full advantage of modern IC processes developed by commercial industry, independent of government funding.

- With access to modern IC processes and CAD tools, the space flight electronic designer can realize a great deal of creativity in the design of future electronics and expect such electronics to be available at reasonable prices
- Along with access to use commercial IC processes and CAD tools comes the ability to utilize available intellectual property (IP) cores.
- Radiation hard technologies often depend on combinations of larger capacitance, resistance, and current sources to overcome SEU . These approaches require more power. The radiation tolerant approach proposed here for SEU immunity depends only on the transistor configuration and hence requires lower power and easily translated to smaller feature sizes.

B. ULP CMOS

The total power consumed in CMOS digital systems has two major components, $P_{TOTAL} = P_{DC}+P_{AC}$, where P_{DC} is the power consumed under quiescent DC conditions and P_{AC} is the power consumed by switching the inherent load capacitances in the circuit. P_{DC} is simply the product of the power supply voltage and the transistor leakage current. P_{AC} is equal to the supply voltage multiplied by the average current needed to charge or discharge the load capacitance. The average current needed to charge a capacitor is equal to the product of the capacitance and the magnitude of the voltage change, which is typically equal to the supply voltage, multiplied by the frequency that the capacitor is charged or discharged. With these substitutions the power equation becomes

$$P_{TOTAL} = (V_{SUPPLY} \times I_{LEAK}) + (V_{SUPPLY} \times I_{CHARGE})$$
$$= (V_{SUPPLY} \times I_{LEAK}) + (V^2_{SUPPLY} \times C_{LOAD} \times F_{CLOCK})$$

When F_{CLOCK} is small, the DC component of power consumption is dominant. In this case it is desirable to minimize I_{LEAK} by manufacturing CMOS transistors with a high threshold voltage. Unfortunately, relatively high supply voltages are then needed to maintain an acceptable level of performance. When F_{CLOCK} is large the AC component of power consumption becomes dominant, and the power consumption of CMOS circuits rivals that of "power hungry" bipolar technologies. Efforts to reduce C_{LOAD} or F_{CLOCK} can achieve significant reductions in power, but reducing V_{SUPPLY} is a much more powerful approach since this term is squared in the AC power component.

However, in order to maintain high level performance at reduced supply voltage, V_{DD} , the transistor threshold voltage, V_T , must be correspondingly reduced. Digital logic typically uses a V_{DD}: V_T ratio of 3:1 to 5:1 for high performance while maintaining adequate noise margins. For a V_{DD} of 500mV this would suggest that a V_T of 100mV to 170mV is needed. Unfortunately, the variation in V_T due to manufacturing, temperature, and other environmental effects is relatively large at these levels and would make it very difficult to design conventional circuits that can be manufactured with high yield and used in a broad range of conditions.

One solution to this problem is to abandon the notion of the transistor threshold as a fixed parameter. By actively controlling the transistor thresholds one can compensate for the variability described above and allow device operation at very low supply voltage. The bias voltage has a polarity that will increase the reverse bias at the source/body junction, such that the body effect increases the operational threshold voltage with increased magnitude of the bias. Thus, the threshold voltage can be controlled in real time during circuit operation.

C. RT ULP

ULP is a unique technology that involves CMOS process modification and circuit design. RT allows SEU and SEL tolerance to be controlled by other circuit techniques. The combination of the technologies can produce low voltage CMOS for space flight use.

In making RT ULP work optimally, not only new electronic circuits must account for increased leakage current; additional back bias voltage generators and I/O interface voltage level shifting circuits are needed for proper ULP circuit operation and interface.

III. PERFORMANCE

The Field Programmable Gate Array (FPGA) is a competing technology that is receiving considerable attention primarily due to ease of implementation. There are serious drawbacks to their use in flight electronics that need to be evaluated and it is beyond this paper to re-iterate past issues. However in recent work in partnership with Los Alamos National Laboratories who were evaluating Xilinix million gate FPGAs for flight use, the following results were just reported[10]. The main issue is providing protection for SEU events, with the primary given to the configuration logic which dominates the FPGA chip area. In the past most attention was given to the computational logic, but since the configuration logic of an FPGA dominates the chip area, this logic is the weak link. The technology of choice for SEU protection is to use Triple Modular Redundancy (TMR). In the above study[10] it was shown that a TMR version of a given design required 4 times the hardware and resulting design is even more sensitive to SEUs than a non-redundant design. A TMR design with better tolerance which includes more complex feedback within triplicated voter systems

result in 6 times the hardware. The approach advanced it the work here has a 2X hardware impact in general[9].

Several sophisticated RT circuits have been developed on the same fabrication process for both 3.3 V and 0.5 V circuits. Two commonly used communication chips are re-engineered: the Reed-Solomon 16-error correction coder and the lossless data compression coder, both conforming to the CCSDS recommendations for space. Both coders had previously been fabricated for 5V or 3.3 V operations and both had been flown on several NASA missions. Electrical performance testing has been conducted on both encoders fabricated on the same process. Several versions of each coder were fabricated using the same mask but with designs targeted for either 3.3V or 0.5V operations. For the compression chip, Fig. 1 provides the power consumption comparison between the 3.3V circuit, 0.5V circuit and a circuit that has 0.5V core but with 3.3V interface.

At 30 MHz clock, the compression chip can process up to 450 Mbps utilizing only 13mW of power, which is over 30:1 power reduction compared to the 3.3 V part. Similar power reduction is obtained on the Reed-Solomon encoder, which at 200 Mbps consumed only 4 mW. To insure a proper comparison, the Reed-Solomon encoder was fabricated with identical mask sets for both the 3.3 volt and 0.5 volt processes, therefore only process changes were reflected in the power reduction measurements.

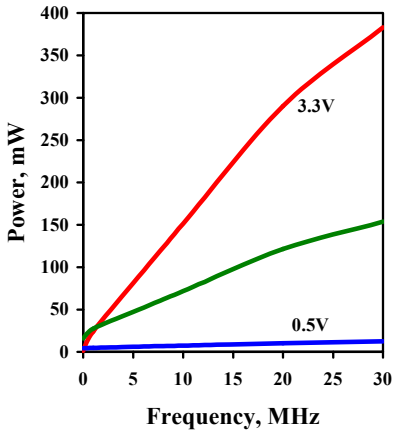

Fig. 1. Measured power consumption for (1). 3.3V part (red), (2). part with 3.3 V pad, 0.5 V core (green) and (3). 0.5 V part (blue).

It is clear from the testing result that the actual performance validates theoretical projection of a power reduction ratio proportional to V^2. However, if level-shifting is required for interfacing with external 3.3V circuit, then half of the power is spent on the interface. The implications of RT ULP are significant and are illustrated in a correlator designed for a GSFC radiometer program; the ECL design required approximately 20 watts whereas a RT ULP design required only 10 mwatts operating at the specified 500 Mhz rate[8].

Several other ULP (RT or non-RT) chips have been developed:

- 8051 micro-controller (RT ULP)
- C50 DSP chip (ULP only)
- 500 Mhz Correlator (RT ULP) for GSFC's radiometer development [4,8]
- Cross correlator RT ULP for the Lightweight Rainfall Radiometer which processes cross-correlation among 25 channels less than 1 watt over 200 Msamples/sec [4].

Radiation tests on the RT ULP Reed-Solomon chip has been performed with satisfactory results [5]. Flight qualification of this chip is in the process of integration for technology demonstration on NASA's ST-5 mission.

IV. POTENTIAL IMPACT ON SPACECRAFT AND SCIENCE

A first direct impact of RT ULP electronics on NASA's missions is reduced requirement for electrical power. For solar energy powered spacecraft, reduction in power translates into smaller solar panel, mass and battery requirements. Secondary effect includes reduced fuel, heat sink, and drag during maneuver. For future solar powered constellation missions, reduced area for body-mounted solar cells will result in smaller spacecraft volume which will allow more craft of the same class to be launched in each lift-off. The domino effect has been studied earlier at Goddard at sub-system levels for the EO-1 mission [6], and at the Applied Physics Labs (APL/JHU) [7] for different classes of missions. These studies uniformly concluded that RT ULP electronics will have a major impact on future spacecraft designs.

The most promising, yet often overlooked potential of RT ULP is its ability to "***enable new science and discovery***". Concepts for synthetically thinned aperture radiometer (STAR) requires onboard processing of multiple channels of received microwave signals to be cross-correlated simultaneously. The amount of processing, if implemented in 3.3 V logic will not permit a single-chip/single-board implementation due to the excessive power consumption necessitating additional hardware for proper heat dissipation. For future deep space missions exploring outer planets, due to the long communication delays, it is foreseeable that onboard radar signal processing and automated processing/reasoning will be needed for situation analysis and quick response. Such processing, if all implemented in 3.3V logic will add considerable mass to the craft, thus limiting what would be implemented. Even though this type

of mission will be using a nuclear power source, the use of ULP logic will definitely alleviate mass/volume constraint.

V. STATUS AND PLANNED FUTURE WORK

Currently the RT ULP technology provides :

- Mature RT ULP digital design at 0.35u CMOS
- Radiation characteristics adequate for near-Earth missions: single event latch-up free, single event upset immunity to near-Earth mission levels with total dose tolerance over 200 krad.

Future work for bringing the technology for infusion in spacecraft sub-systems will require:

- Complete on-chip automatic back-bias generation mechanism for RT ULP circuits. Current circuits required two additional power supplies at different levels to bias the transistors.
- Complete radiation tests on earlier fabrication runs and validating RT ULP library. The Reed-Solomon (RS) and the compression encoders were re-engineered for RT ULP utilizing two different circuit design methodologies. While the RS chip has been fully radiation tested, the compression encoder needs to be tested to fully characterize the design library.
- Develop mixed analog/digital RT ULP methodology
- Developing RT ULP for 0.25u and possibly 0.18u as CMOS feature size decreases
- Developing RT ULP processors for commonly required onboard processing needs such as Analog-to-Digital Converter (ADC), data transmission protocol (e.g. spacewire), base-band modulator, FPGA, DSP, etc.
- RT ULP CPU processors are needed to meet the general purpose computation requirement for spacecraft. Potentially a range of processors could be implemented to meet various needs. Low computational needs could be met with a General Dynamics V-20 processor and high end processing could perhaps be met with a LEON design, which is a 32-bit SPARC V6 CPU.
- Memory needs to be created for at least two classes of problems: 1) Small memories which are embedded within special purpose processors; these memories are configured in various width and depth depending on the application. These could be implemented with SEU immune storage cells without error correction[11]. 2) Large general purpose memories cannot use SEU immune storage cells efficiently and therefore must utilize a non-SEU tolerant cell with error correction.
- Investigating the *ultra low temperature* (ULT) characteristics of the RT ULP circuits.
- Developing spacecraft low power conversion, including dc-to-dc converters, and distribution components

New designs need to implement more sophisticated algorithms into future NASA data processing requirements. Higher performance specifications require higher density electronics which imply the use of smaller feature size processing. For example, the Goddard Bit Plane Encoder (BPE) processor will not fit in the current 0.35 micron RT ULP feature size devices. Too many transistors are needed. An RT 0.25 micron TSMC process is being used to implement the BPE. A major problem has surfaced however. In normal CMOS processing, there is a direct correlation between density and feature size. However, radiation tolerant designs have a critical factor that can be ignored in non-space environs. The dominant design element in RT electronics is the critical node minimum distance parameter where certain charged nodes must be partitioned to meet a minimum distance requirement. The distance is largely independent of the feature size. With micron feature size (> 1 micron) processing, this distance is dominated by the transistor layout rules and therefore have a minimal effect. However, for deep submicron processing (<0.25), the critical node distance dominates layout. The implication of this situation is that the use of standard cell libraries will be grossly inefficient. For example, a first order calculation where the critical node distance is 25% the size of a cell, the layout efficiency is 44%. If the critical node distance is 50% of the size of a cell, the layout efficiency is only 22%. Clearly, a new foundation is needed for automated RT VLSI synthesis.

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